REMARKS

We are in receipt of the Office Action dated March 12, 2001, and the above Amendment and following remarks are made in light thereof.

Claims 1, 3, 15, 18, 21, 2 and 27-55 are pending in this application, with claims 35-41 and 50-55 having been withdrawn from consideration as being drawn to a non-elected species. In the Office Action each of claims 1, 3, 15, 18, 21, 24, 27-34 and 42-49 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al., U.S. Patent 5,893,740, in view of Ko et al., U.S. Patent 5,686,321, and Mikoshiba, JP 56-060061.

The present invention is characterized in a semiconductor device formed in a single semiconductor substrate, wherein an impurity is introduced from a perpendicular direction to a plane having the smallest atomic density of the single semiconductor substrate, as required by amended claims 1, 29 and 42.

In the rejection, the Examiner recognizes that Chang et al. do not "disclose that the impurity is introduced from a direction of the <110> axis with respect to the single semiconductor substrate, " but contends that the impurity doping direction in Chang et al. is inherently along the <110> direction. Applicant does not agree that Chang et al.'s IC device can be presumed to be inherently along the <110> direction merely because it is old and well known in the art that the MOSFET are normally formed with the wafer surface being parallel to the (100) crystal plane and with the channel being commonly aligned to <100> crystal direction, as described in Mikoshiba.

The important concept of the present invention is that the impurity ion is added from the direction perpendicular to the plane of the silicon substrate, at which the atomic density is the smallest (see the specification at p. 9, lns. 15-17). In neither Chang et al. nor Mikoshiba is it noted that the impurity ion is added from the angle that is the least likely to damage to the silicon substrate (see the specification

at pp. 4, lns. 8-10), which is the <110> axis, since silicon has the smallest atom density on the {110} face (see the specification at p. 4, lns. 11-13).

Mikoshiba discloses that the piezo effect is minimized by coinciding the channel direction of a P type channel field effect transistor with <100> direction (abstract). Thus, Mikoshiba does not note the damage and the smallest density.

In addition, although Ko et al. teaches the concentration of the punchthrough stopper regions, the reference is not related to the implantation direction.

Accordingly, Applicant believes that, pursuant to the foregoing Amendment, the application is in condition for allowance, and an early Office Action in this regard is earnestly solicited.

Respectfully submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of	)
Akiharu MIYANAGA et al.	)
Serial No.: 09/241,695	)
Filed: February 2, 1999	)
For: Semiconductor Device And Process For Producing The Same	)
Art Unit: 2811	)
Examiner: S. Hu	)

Commissioner for Patents
Washington, D.C. 20231

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Please amend claims 1, 29 and 42.

1. (Amended) A semiconductor device comprising a plurality of MOSFETs formed in a single semiconductor substrate,

each of the plurality of MOSFETs comprising:

a source region and a drain region each including a first impurity;

a channel forming region being formed between the source region and the drain region; and

an impurity region including a second impurity having an opposite conductive type to the first impurity and being formed under the channel forming region,

wherein a concentration of the second impurity in the channel forming region is from 1/100 to 1/10 of that in the impurity region,

wherein the second impurity is introduced from a direction of the < 110 > axis with respect to the single semiconductor substrate, so that the second impurity is introduced from a perpendicular direction to a plane having the smallest atomic density of the single semiconductor substrate,

wherein the concentration of the second impurity in the impurity region is in a range of 1×10^{18} to 1×10^{19} atoms/cm^3,

wherein the concentration of the second impurity in the channel forming region is in a range of 1×10^{16} to 1×10^{17} atoms/cm^3.

29. (Amended) A semiconductor device comprising a plurality of MOSFETs formed in a single semiconductor substrate,

each of the plurality of MOSFETs comprising:

a source region and a drain region each including a first impurity;

a channel forming region being formed between the source region and the drain region;

an impurity region including a second impurity having an opposite conductive type to the first impurity and being formed under the channel forming region;

a pair of LDD regions, wherein one of the pair of LDD regions is formed between the source region and the channel forming region while the other of the pair of LDD regions is formed between the channel forming region and the drain region,

wherein a concentration of the second impurity in the channel forming region is from 1/100 to 1/10 of that in the impurity region,

wherein the second impurity is introduced from a direction of the < 110 > axis with respect to the single semiconductor substrate, so that the second impurity is introduced from a perpendicular direction to a plane having the smallest atomic density of the single semiconductor substrate,

wherein the concentration of the second impurity in the impurity region is in a range of 1 x 10^{18} to 1 x 10^{19} atoms/cm^3,

wherein the second concentration of the impurity in the channel forming region is in a range of 1 x 10^{16} to 1 x 10^{17} atoms/cm^3.

42. (Amended) A semiconductor device comprising at least a CMOS circuit including an n-channel MOSFET and a p-channel MOSFET each being formed in a single semiconductor substrate,

said n-channel MOSFET comprising:

a first source region and a first drain region each comprising a first n-type impurity;

a first channel forming region being formed between the first source region and the first drain region;

a first impurity region including a first p-type impurity and being formed under the first channel forming region;

said p-channel MOSFET comprising:

a second source region and a second drain region each comprising a second p-type impurity;

a second channel forming region being formed between the second source region and the second drain region;

a second impurity region including a second n-type impurity and being formed under the second channel forming region,

<u>wherein each of the first and second impurities is introduced from a perpendicular direction to a plane having the smallest atomic density of the single semiconductor substrate,</u>

wherein a concentration of the first p-type impurity in the first impurity region is in a range of 1 x 10^{18} to 1 x 10^{19} atoms/cm^3,

wherein a concentration of the first p-type impurity in the first channel forming region is in a range of 1×10^{16} to 1×10^{17} atoms/cm^3

wherein a concentration of the second n-type impurity in the second impurity region is in a range of 1×10^{18} to 1×10^{19} atoms/cm^3,

wherein a concentration of the second n-type impurity in the second channel forming region is in a range of 1×10^{16} to 1×10^{17} atoms/cm^3.